We claim:

1. A method for fabrication of silicon-on-nothing (SON) MOSFET using selective etching of $Si_{1-x}Ge_x$ layer, comprising:

preparing a silicon substrate;

growing an epitaxial $Si_{1-x}Ge_x$ layer on the silicon substrate;

growing an epitaxial thin top silicon layer on the epitaxial $Si_{1-x}Ge_x$ layer;

trench etching of the top silicon and $Si_{1-x}Ge_x$, into the silicon substrate to form a first trench;

selectively etching the $Si_{1-x}Ge_x$ layer to remove substantially all of the $Si_{1-x}Ge_x$ to form an air gap;

depositing a layer of SiO_2 by CVD to fill the first trench;

trench etching to from a second trench;

selectively etching the remaining $Si_{1-x}Ge_x$ layer;

depositing a second layer of SiO_2 by CVD to fill the second trench, thereby decoupling a source, a drain and a channel from the substrate; and

completing the structure by state-of-the-art CMOS fabrication techniques.

2. The method of claim 1 wherein the thickness of $Si_{1-x}Ge_x$ is less than the critical thickness of $Si_{1-x}Ge_x$ so that no relaxation occurs and no defects form in the $Si_{1-x}Ge_x$ layer, and is between about 3 nm and 50 nm.

3. The method of claim 1 where the etching time is controlled during the first etching step so that some SiGe remains on the smallest features of the structure to prevent lifting of the top silicon layer.

4. The method of claim 1 wherein said growing an epitaxial $Si_{1-x}Ge_x$ layer on the silicon substrate includes growing a $Si_{1-x}Ge_x$ layer having a Ge content of between about 10% to 80%.

5. The method of claim 1 wherein said growing an epitaxial thin top silicon layer, on the epitaxial $Si_{1-x}Ge_x$ layer includes growing a silicon layer having a thickness of between about 3nm to 100nm.

6. A method for fabrication of silicon-on-nothing (SON) MOSFET using selective etching of $Si_{1-x}Ge_x$ layer, comprising:

preparing a silicon substrate;

growing an epitaxial $Si_{1-x}Ge_x$ layer on the silicon substrate, wherein the thickness of $Si_{1-x}Ge_x$ is less than the critical thickness of $Si_{1-x}Ge_x$ so that no relaxation occurs and no defects form in the $Si_{1-x}Ge_x$ layer;

growing an epitaxial thin top silicon layer on the epitaxial $Si_{1-x}Ge_x$ layer;

trench etching of the top silicon and $Si_{1-x}Ge_x$, into the silicon substrate to from a first trench;

selectively etching the $Si_{1-x}Ge_x$ layer to remove substantially all of the $Si_{1-x}Ge_x$ to form an air gap;

depositing a layer of SiO_2 by CVD to fill the first trench;

trench etching to from a second trench;

selectively etching the remaining $Si_{1-x}Ge_x$ layer;

depositing a second layer of SiO_2 by CVD to fill the second trench, thereby decoupling a source, a drain and a channel from the substrate; and

completing the structure by state-of-the-art CMOS fabrication techniques.

7. The method of claim 6 where the etching time is controlled during the first etching step so that some SiGe remains on the smallest features of the structure to prevent lifting of the top silicon layer.

8. The method of claim 6 wherein said growing an epitaxial $Si_{1-x}Ge_x$ layer on the silicon substrate includes growing a $Si_{1-x}Ge_x$ layer having a Ge content of between about 10% to 80%.

9. The method of claim 6 wherein said growing an epitaxial thin top silicon layer, on the epitaxial $Si_{1-x}Ge_x$ layer includes growing a silicon layer having a thickness of between about 3 nm to 100 nm.